

A Test Microchip for Evaluation of Hermetic Packaging Technology for Biomedical Prosthetic Implants

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Abstract—The development of a test chip that will be used to evaluate a hermetic and biocompatible package for the driving CMOS circuitry of a retinal prosthesis is described. The package design is estimated to be about 2 x 2 x 0.3 mm³ and will be formed by conformal layers of parylene and a metal (e.g. titanium) as inner and outer protections, respectively. The test chip has been specifically designed for evaluation of the packaging technology. It consists of many blocks of analog and digital components as well as relative humidity and temperature sensors. The test chip has more probe points than a typical chip, allowing a more thorough evaluation of circuit behavior during the testing. This chip will first be coated in a layer of parylene C and soaked in heated isotonic saline for an extended period of time. Every block in the chip will then be tested for functionality using the surface probe points. The next step is to coat the surface of another test chip with parylene and a metal and repeat these soak tests. The results will then be analyzed and mean time-to-failure for the different samples will then be computed. Using the accelerated testing paradigm, these results will then be extrapolated to mean time-to-failure in the operating intraocular environment. Parylene test structures have already undergone an accelerated lifetime test and results have been analyzed.

Keywords— Hermetic packaging, soak testing, test chip, biomedical implants.

I. INTRODUCTION

Suitable packaging of implantable biomedical devices and circuitry poses a great challenge for designers because not only do the devices need be protected from the body's fluids and remain fully functional, but the body also needs to be well protected from the materials used in the devices. These materials should not in any way harm the tissue. Hermetic packaging thus serves as a protective barrier both for the devices and for the body. Depending on the needed lifetime of packages used in a specific application, a variety of schemes have been used to encapsulate biomedical devices [1]. Polymers like parylene C have already been used for cases when the required life-expectancy was relatively short [2].

This paper describes a test microchip that has been designed that can be used in testing of hermetic packages exposed to moisture. This test chip will give a better sense

of life expectancy of biomedical circuitry in harsh environments like the human body.

II. METHODOLOGY

A. Test chip

An older generation test chip that was previously designed and fabricated could not easily be implemented in these hermetic packaging tests several reasons. The inputs and outputs were not easily accessible in this old scheme. Also, there were only two probe points available to check for failure/functionality. The new test chip has somewhat different functionality than the real chip that will be used for retinal stimulation. This chip is designed mainly for hermeticity testing purposes. The test chip includes the representative circuits needed for a 1000 channel retinal prosthesis, but it need not have 1000 channels of output. It also has many probe points available to check the functionality. This test chip is being developed to study the long-term effect of moisture on electronic devices. It consists of simple blocks such as CMOS inverter, P-N Junctions, Differential Amplifiers, and Capacitors. It is built using AMI 1.5 μ m bulk CMOS technology. It is approximately 2 mm x 2 mm with many probe points for measuring the functionality of each component. Figure 1 depicts the layout for the test chip.

On the chip there are also several inter-digitated combs of metals placed in between the electronic components. These dew point sensors have previously been used for lifetime testing of hermetic packages [3] [4]. These metals are used as moisture sensors. These sensors are placed along interconnects especially on locations that moisture can easily penetrate and also inside the chip. This is usually where the metal sealing ends. When moisture penetrates through these combs, it changes the capacitive and resistive properties of these metals. By real-time monitoring the output of the chip and the resistive and capacitive change of the moisture sensors, a relationship can be found between impedance changes in the moisture sensor and the time it takes for the chip to fail.

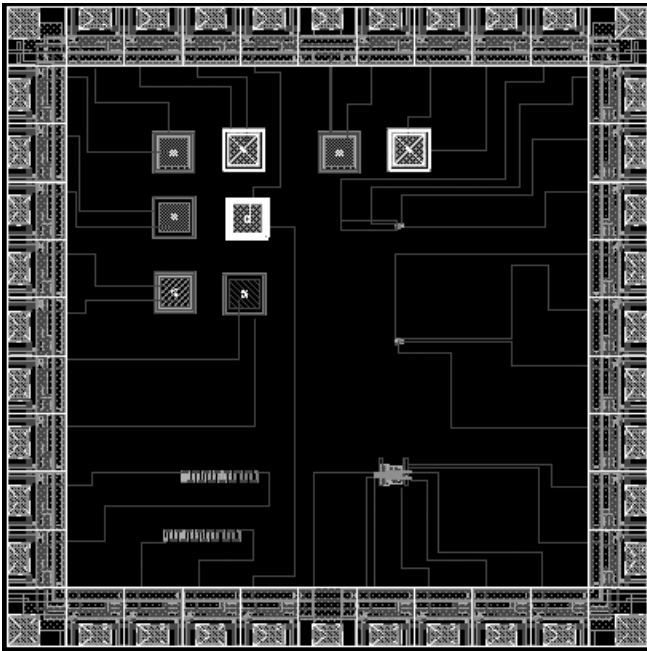


Figure 1. A layout of the test chip

B. Package Structure

For the first test samples, parylene C is deposited on the test chip. A significant advantage of the use of parylene is its conformality. After the chip has been uniformly covered in parylene, the samples can undergo soak tests. The second group of test samples is initially treated in exactly the same manner. After this parylene deposition, an external layer of metal, titanium for instance, is evaporated or sputtered on the surface. This metallized group of test chips can now undergo a similar soak test.

C. Test Procedure

Under the accelerated testing paradigm, soak testing is performed at a temperature higher than its end-use temperature because experiments have shown that for every 10°C raise in temperature, the lifetime of the device being tested will be approximately divided by half [5].

In order to get a better sense of the failure modes of the test chip, a very simple test can be performed. Untreated test chips will be immersed in saline solution under this accelerated testing scheme and analyzed consistently for component failure. Using the probe points already built on the chip, each component in the chip can be easily tested for lost functionality. It is essential to determine these failure modes early so that they can be detected if they occur when the chip is encapsulated in its hermetic package. The test chips covered by parylene are then soaked in saline solution at the same temperature and evaluated for component failure after a specified time (making contact to the probe points

destroys the hermetic seal). The chips encased in both parylene and metal are then soaked and tested in a similar manner.

After these tests have been performed, it is possible to extrapolate mean time-to-failure (MTTF) at the operating temperature. By comparing these MTTF's for the different encapsulation techniques, a thorough analysis can be completed on the test chip life-expectancy under the different packaging schemes.

III. RESULTS

The design for the test chip has been completed and it is ready for fabrication. The die size is approximately 2 x 2 mm². It includes 40 I/O pads, eleven different blocks of analog and digital components, and many probe points on top.

Parylene coated metal lines have undergone heated (55°C) isotonic saline soak tests for a period of five months and the data from these tests have shown that the impedance of these lines did not change significantly during this period of time. These results suggest that parylene itself will likely serve as an excellent barrier to water and salt penetration for the CMOS circuitry.

However, by using a metal as the outer protective layer of the package, the permeability of the package to moisture will likely be much less. It is estimated that by using a combination of metal and parylene, the package can remain intact *in vivo* for over 10 years [6]. These data are shown in Figure 4. Similar soak testing of the test chip will start shortly to determine the MTTF of the test chip.

IV. CONCLUSION

We have designed a test chip as well as a testing procedure for further development of a robust hermetic sealing technique. We aim to define the failure modes of the CMOS circuitry implemented in the driver chip for the retinal prosthesis and determine how to prevent these failures through development of a hermetic sealing technology. Parylene is likely a good choice for initiation of a hermetic seal because of its conformality. Metal is also usually a very important material in hermetic packages because of its low permeability to moisture. The advantages of each will be determined through the use of these test chips.

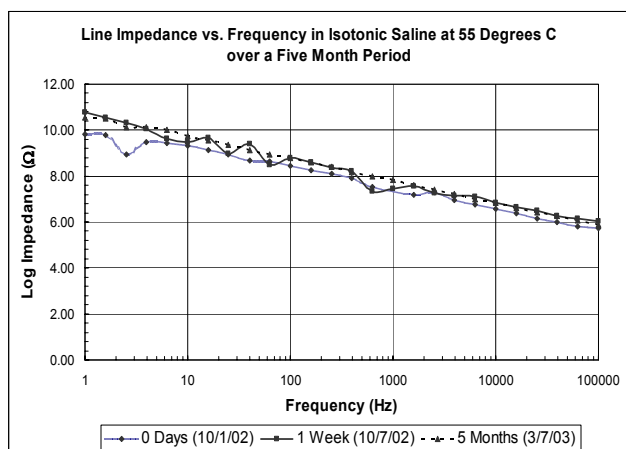


Figure 3. Impedance of parylene coated lines as a function of frequency over a five month period

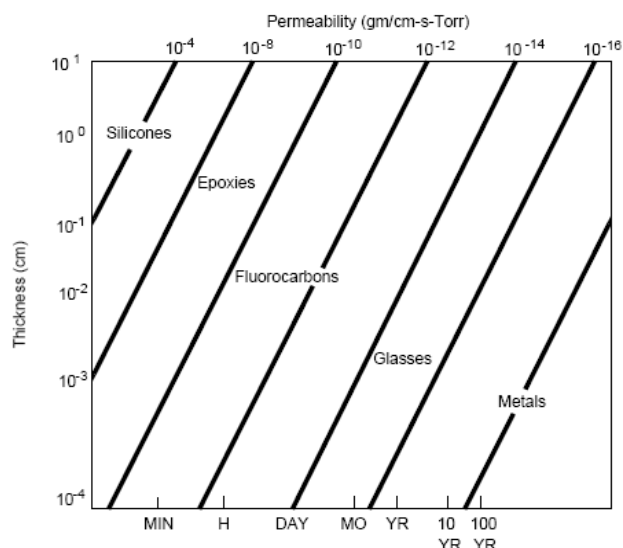


Figure 4. Permeability vs. time of different materials

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